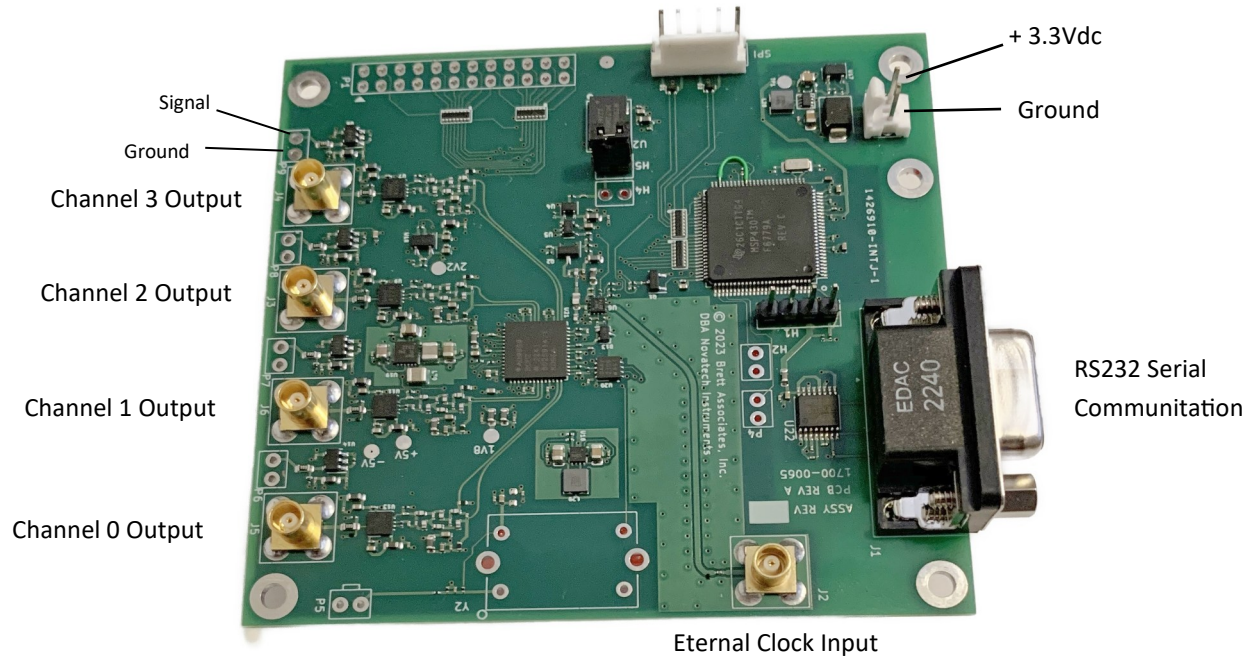


NOVATECH INSTRUMENTS

INSTRUCTION MANUAL

Model DDS9m, 171 MHz, 4-Channel Signal Generator Module



Model DDS9m

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1.0 DESCRIPTION

1.1 The Model DDS9m is a four-channel Direct Digital Synthesizer (DDS) on a small printed wiring module with RS232 serial control. The DDS9m provides four independent sine wave and LVCMOS output signals, which can be set from 0.1Hz to 171MHz in 0.1Hz steps when using the internal TCXO clock (LVCMOS is optimized for outputs greater than 1MHz and less 125MHz).

1.2 The DDS9m can also be used with an External Clock input. An on-board programmable frequency multiplier generates the master clock allowing user configured frequency ranges. The multiplier can be disabled for direct inputs up to 500MHz for optimum phase noise performance. When used with the same external clock source, multiple DDS9m are phase synchronous.

2.0 SPECIFICATIONS

2.1 OUTPUTS

TYPES: Four Sine and LVCMOS simultaneously (four frequencies.)

IMPEDANCE: Sine: 50 Ω ; LVCMOS: 50 Ω . **RANGE:** 0.1Hz to 171MHz in 0.1Hz steps (Sine out, int. clock).

SINE AMPLITUDE: approximately 1V_{pp} (+4dBm @ 35MHz) into 50 Ω . Programmable from 0/1024 to 1023/1024 of Full Scale (10-bits).

PHASE: Each channel 14-bits programmable.

FLATNESS: ± 3 dB from 1kHz to 150MHz referenced to amplitude at 35MHz, full scale.

2.2 LVCMOS AMPLITUDE

$V_{oh} \geq 2.4V$ and $V_{ol} \leq 0.4V$ when series terminated. Rise and fall times $< 1.5ns$. (1MHz $< F_{out}$ $< 125MHz$)

2.3 CONTROL

Output frequencies, amplitudes (10-bits) and phases (14 - bits) are controlled by an RS232 serial port at 19.2kbaud. All settings can be saved in non-volatile memory.

2.4 ACCURACY AND STABILITY

Accuracy: $< \pm 1.5ppm$ at 10 to 40°C. Stable to an additional $\pm 1ppm$ per year, 18 to 28°C. (internal clock)

2.5 EXTERNAL CLOCK IN

LEVEL: 0.2 to 0.5V_{rms} Sine or Square Wave. 50 Ω .
FREQUENCY: 10MHz to 125MHz with multiplier of 4 to 20 enabled. Direct input of 1MHz to 500MHz.

2.6 SPECTRAL PURITY (Typ. 50 Ω load, internal clock, full-scale output)

Phase Noise: $< -120dBc$, 10kHz offset, 5MHz out.

Spurious: (typ. 300MHz span)

$< -60dBc$ below 10MHz

$< -60dBc$ below 40MHz

$< -55dBc$ below 80MHz

$< -50dBc$ below 160MHz Harmonic:

$< -65dBc$ below 1MHz

$< -55dBc$ below 20MHz

$< -45dBc$ below 80MHz

$< -35dBc$ below 160MHz

(channel-channel isolation: $< -60dBc$)

2.7 TABLE MODE

On-board memory holds up to 32,768 profile points in table mode allowing a different output in 100 μs increments. Channels 0 and 1 only.

2.8 POWER REQUIREMENTS

+3.14V to +3.46VDC@,750mA.

2.9 SIZE

82.6mm by 88.9mm circuit board. Max. height 10mm.

2.10 CONNECTORS

MCX for Sine Outputs and EXT CLK IN. 2-pin header for +3.3V power. DE9 for Serial Control. 2-pin wire points for LVCMOS outputs.

3.0 HARDWARE INSTALLATION

WARNING

The DDS9m contains static sensitive components. Before opening the package, follow appropriate static precautions. Failure to follow static precautions may damage the DDS9m.

3.1 Power Connection. Power of +3.3Volts DC is applied through a 2-pin connector (mates with Amp 640441-2). See cover photo for location of the connector. If you are using a Novatech Instruments sup-

plied connector, Red is +3.3VDC and Black is the common return.

3.2 The quality of your power supply may affect the performance of the DDS9m. The supply should be free of ripple and noise (<50mV). Even though extensive filtering is used on the DDS9m board, a quiet and well regulated power supply will ensure optimum performance. If switching power supplies are used, please verify that your system noise requirement is met.

3.3 RS232 Communication. To use the DDS9m in the RS232 mode, connect your host computer to the 9-pin female RS232 connector on the DDS9m. If you are using a PC, a 9-pin monitor extension cable used as an RS232 cable will allow direct connection to the DDS9m without the use of a null modem cable or gender changer. If you are using a different computer, terminal or other control source, please note that the data **TO** the DDS9m is on pin 3; the data **FROM** the DDS9m is on pin 2 and the **COMMON** return is on pin 5. Set your host to 19.2 kbaud, 8 bits, 1 stop bit, no parity and no hardware flow control. See Table 1 for RS232 Serial Commands.

3.4 You may use a USB to RS232 adapter cable with computers that do not provide a serial port. Follow the manufacturer's installation instructions when using a USB adapter.

3.5 Commands are not case sensitive. There must be a space after each command except R, CLR, S and QUE. End with any combination of CR, LF or CRLF. Illegal commands will result in a ?0 error code being returned

3.6 QUE Command. The "QUE" command returns five hexadecimal strings reflecting the present state of the DDS9m. An example of the response to a QUE command follows:

NOTE:

The windows application SOF8_409 is available for the DDS9m. This program provides a graphical interface that displays the results of the QUE command in decimal numbers and allows simple control of the DDS9m.

3.7 SPI Communication. Contact the factory for information on using the Serial Peripheral Interface with the DDS9m.

3.8 Internal Clock. If you plan to use the DDS9m internal clock, which is the factory default mode, no action is

Example for QUE Command

05F5E100 0000 03FF 0000 00000000 00000000 000301
05F5E100 1000 03FF 0000 00000000 00000000 000301
05F5E100 0000 03FF 0000 00000000 00000000 000301
05F5E100 1000 03FF 0000 00000000 00000000 000301
80 BC0000 0000 6102 21
<p>Description (All values above are in hexadecimal): The lines above describe current settings for the four output channel numbers 0,1,2 and 3 in sequence. For example, Channel 0 values are: "05F5E100" = frequency in 0.1Hz steps per LSB (10MHz); "0000" = phase setting (0); "03FF" = amplitude setting(1023). The last four groups of hex values on the first four lines and the entire last line describe AD9959 and microcontroller register settings for use by the factory.</p>

required. If the DDS9m was previously set to use the external clock, send the serial command "C i" to reselect the internal clock. If you wish to maintain this setting, use the save command "S".

3.9 External Clock. If you are providing your own clock source, send the serial command "C e". Apply your clock to the External Clock Input MCX. Note that phase noise and stability are dependent upon your supplied clock. See specifications for signal levels required and acceptable frequency range. If you wish to maintain this setting, use the save command "S".

3.10 The external clock can also be used with Kp=1 for direct connection to the DDS generator. With Kp=1, the PLL multiplier is disabled. Use this direct input, up to 500MHz, for optimum phase noise performance

NOTE:

When using an external clock, frequency scaling of the "Fn" command may be required. Please see Operation, Section 4, for details

3.11 Signal Outputs. There are eight signal outputs on the DDS9m: four channels of Sine and the corresponding LVCMOS/TTL. The Sine outputs are provided on MCX connectors (Johnson Components, 133-3701-133 or equivalent) on the board edge. Simply connect your 50Ω application cable to appropriate output. The LVCMOS outputs are on wire points near the MCX outputs. The pad closest to the MCX connector is the ground and the other pad is the signal output.

3.12 Mounting. Five mounting holes are provided on the board. These holes are electrically connected to circuit common and may be used for shield connections. Clearance is provided for up to 3mm diameter screws. Please allow at least 3 mm clearance on the bottom side when mounting to a conductive chassis or case.

3.13 Mounting Holes. The DDS9m has PCB mounting holes with center positions spaced 3.20” left to right and 2.90” top to bottom as shown on the photo on the first page of this manual. These holes are electrically connected to circuit common.

3.14 Interface Connector P1. Active Pins are 1 and 3 (power supply common), pin 2 (3.3V power supply reference, 50mA max), pin 10 (TS Control input) and pin 14 (IOUD input/output). An arrow on the board points to pin 1 as shown on the top left corner of the cover photo. Odd numbered pins are on the bottom row and even numbered pins are on the top row. Contact factory for information on the other even pins.

WARNING:

The P1 input pins are 3.3V CMOS compatible. Applying 5V logic signals to these inputs will permanently damage the DDS9m.

NOTE:

The DDS9m is cooled by convection. Verify that there is adequate free air flow around the board when mounting in an enclosure. Approximately 2 Watts are dissipated.

4.0 Operating Instructions

4.1 Power on reset. After power is applied, the DDS9m takes approximately 500ms to initialize. Commands sent during this time will be ignored or may cause erroneous operation.

4.2 Specifications are met within 15 minutes of power-up in stable environment

4.3 After the DDS9m has been installed in the customer application system, all that is required for operation is to send the appropriate serial commands per Table 1 on the last page.

NOTE

The “B” command shown in Table 1 can be used to test the AD9959 DDS chip programming as it allows access to all internal registers. While not a real-time simulation, each “B” command functions as an input by putting a data byte directly into the AD9959 via an SPI port, and then pulses the IOUD line. This is similar to a procedure that a customer control circuit might perform. The “B” command values are not saved so they will not show in the Q or QUE command output. Consult the Analog Devices for support. Novatech Instruments does not provide tech support for the “B” command.

4.4 The user host computer software must properly format the serial commands. Incorrect formatting will result in an error code being returned.

4.5 For maximum interface speed, it is suggested that Echoing be disabled by the “E d” command. This will allow the host to send characters at a faster rate. Note that no flow control is provided. Depending upon your host, the DDS9m may not be able to keep up with serial characters. The DDS9m will respond with an “OK” for a correctly received data command. You will have to verify correct operation at your host rate.

4.6 Special baud rate commands are available if you wish to set a different baud rate. Contact the factory for more details.

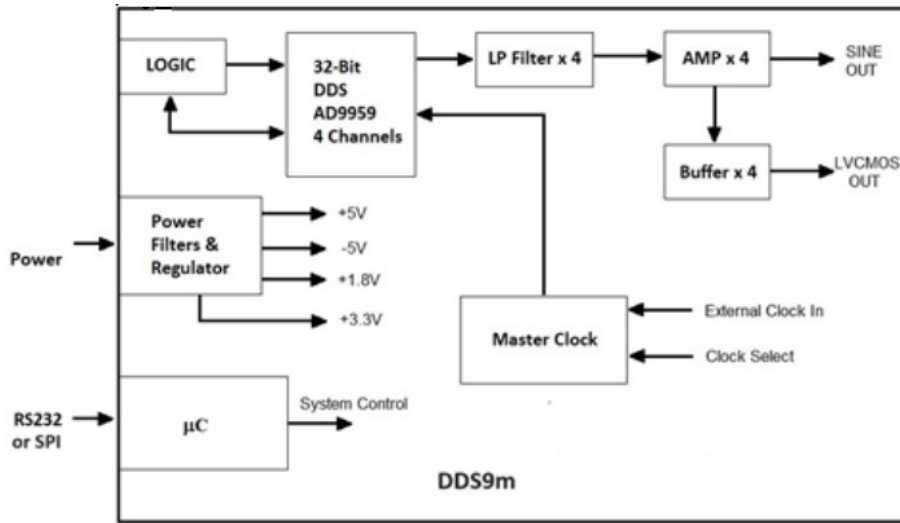


Figure 1
Simplified System Block Diagram

4.7 If you are using an external clock, the value sent to the DDS9m in the “Fn” command must be scaled. The output frequency of the DDS9m when used with an external clock is given by:

$$F_{\text{out}} = (F_{\text{command}}) * (K_{\text{pe}} * F_{\text{ext clk}}) / (K_{\text{pi}} * F_{\text{int clk}})$$

Where K_{pe} is the value of K_{p} set by the user, and K_{pi} is the internal default K_{p} which is 15.

4.8 The nominal Internal Clock has a value of 28,633,115.306666667Hz. Best performance is obtained when the External Clock input frequency times the Reference PLL multiplier (K_{p}) is close to the default value (429.4967296MHz, max: 500MHz), as the on-board low-pass filters are optimized for that range.

4.9 For an example, assume an external clock of 10MHz is used and an output of 1.544 MHz is desired. Also assume a K_{p} of 15. Then:

$$F_{\text{command}} = (1.544) * (15) * (28,633,115.306666667) / (15) * (10,000,000) = 4.4209530$$

The command that is then sent to the DDS9m will be:

Fn 4.4209530

where ‘n’ is your selected channel

NOTE:

You must account for your clock frequency error and calculation roundoff when using an external clock.

4.10 For normal operation the K_{p} command is unmodified. However, if it is desired that the clock multiplier gain bit be set HIGH (for $K_{\text{p}} * [\text{Ext Clk Freq}]$ from 255 and 500 MHz), add hexadecimal 0x80 to the K_{p} value to be set. For the bit to be forced LOW (100 to 160 MHz), add hexadecimal 0x40 to the K_{p} value to be set.

4.11 Since the resolution of the DDS9m is 32-bits, the typical fractional frequency error ($\Delta f/f$) for output frequencies in the MHz range will be less than 0.1ppm, even when exact values are not possible.

4.12 Phase relationships are maintained by appropriate use of the “M” and “I” commands. The “M” command has special modes “M a” and “M n”. “M a” means automatically clear phase at the end of each command. This will clear the phase register each time any command is performed. This is important when all outputs must be phase aligned. However, it may cause a phase discontinuity in the output.

4.13 The “M n” command turns off the automatic clearing of the phase register. This is the default mode. In this mode, the phase register is left intact when a command is performed. Use this mode if you want frequency changes to remain phase synchronous, with no phase discontinuities.

4.14 Further control of phase relationships and timing of command execution can be exercised by using the “I m”, “I a” and “I p” commands. The default mode is “I a” in which a command is parsed and executed immediately following the end of the serial input sequence. In the “I m” mode, an update pulse will not be sent to the DDS chip until an “I p” command is sent. This is useful when it is important to change all the outputs to new values simultaneously.

4.15 For applications which require precise amplitude matching between the channels, the recommended method is to use the “Vn N” command to adjust the channels to match the other. This command provides 10-bits of adjustment range.

5.0 Theory of Operation

5.1 Please refer to the simplified System Block Diagram in Figure 1 for the following discussion.

5.2 At every cycle of the DDS9m master clock, the 32-bit DDS integrated circuit increments the phase of an internal register by a value determined by the frequency setting loaded into the on-chip registers. This digital phase value is converted on-chip to a sinusoidal amplitude level and delivered to on-chip 10-bit digital-to-analog converters. The analog signals from these converters are filtered by differential 7th-order elliptical low pass filters, amplified and sent to the MCX connectors.

5.3 The frequency generated by the DDS IC is determined by the 32-bit frequency word loaded into the frequency register on the DDS9m. The output frequency is given by:

$$F_{out} = F_{setting} * K_p * F_{clock} / 2^{32} \text{ Hz}$$

Where:

$$F_{clock} = 28,633,115.306666667 \text{ Hz (int.)}$$

$$F_{setting} = \text{Binary value in DDS IC.}$$

$$(F_{setting} \text{ ranges from } 0 \text{ to } 2^{31}-1)$$

$$K_p = \text{PLL Multiplier (1 or 4 to 20)}$$

This reduces to:

$$F_{out} = F_{setting} \text{ MHz}$$

for the default clock and $K_p=15$.

5.4 Since the DDS IC is a sampled data system, the output frequency is limited to a maximum of 1/2 the system clock frequency ($F_{setting} \leq 2^{31}-1$). While it is possible to generate an output near 50% of the clock, the distortion may be unacceptable. Therefore, the output is limited to approximately 40% of the system clock and steep output filters are provided on board: in this case 7th-order elliptical low pass filters.

5.5 If you are using an external clock and a K_p which give a clock substantially lower than the 429.497MHz default internal clock, you may need to filter the outputs to obtain acceptable distortion for your application. For best performance, set the corner frequency at 40% or less of your external clock frequency times K_p . The lower your filter as a percentage of your clock frequency, the lower the distortion.

NOTE:

Since filtering occurs before the signal is level shifted to LVCMOS, the LVCMOS outputs may be erratic or distorted when using low clock frequencies. If you require an LVCMOS level signal when using low clock frequencies, it is recommended that you use an external comparator or level shifter connected to the output of your external filter.

5.6 For example, if you are using a 10MHz external clock, with the default reference multiplier (K_p) of 15, then the internal clock is 150MHz. An optimal filter for this frequency would then be approximately 60MHz (40% of 150MHz).

NOTE:

Your value of K_p times your selected clock frequency must not be between 160MHz and 255MHz. For the internal clock, values of K_p from 5 to 9 should not be used. You may also need to set the “VCO gain control” bit. See paragraph 4.10.

6.0 PERFORMANCE TEST

6.1 Install the DDS9m as directed in Section 3. Connect your host controller and operate the DDS9m per Section 4. The test limits assume a stable environment of 18-28°C.

NOTE:

Allow the DDS9m to warm up for at least 15 minutes before performing any measurements. For best results, the DDS9m should be verified in its installed environment.

6.2 See the following list of recommended test equipment to perform the following measurements.

ITEM	SPECIFICATION
Oscilloscope	300MHz, 50 Ohm
Frequency Counter	180MHz
Counter Time Base	10MHz $\leq \pm 0.1\text{ppm}$
External Clock Source	400MHz to 500MHz

6.3 Verify Frequency Accuracy. To verify the frequency of the DDS9m, set the output sequentially to each value in the Frequency Test Point list below, with the clock source set to internal. Connect the recommended frequency counter set to 50Ω termination and 0.1Hz resolution. Verify the limits show. Test all channels to verify functionality of all outputs. If you do not use an external reference for the frequency counter, be sure to add the error of your counter to the tolerance. LSD = Least Significant Digit on counter

Frequency Test Points

FREQUENCY	TOLERANCE
100 kHz	$\pm 0.15 \text{ Hz} \pm 1 \text{ LSD}$
1 MHz	$\pm 1.5 \text{ Hz} \pm 1 \text{ LSD}$
10 MHz	$\pm 15 \text{ Hz} \pm 1 \text{ LSD}$
100MHz	$\pm 150 \text{ Hz} \pm 1 \text{ LSD}$
150MHz	$\pm 225 \text{ Hz} \pm 1 \text{ LSD}$

6.4 Sine Out Amplitude Verification. Set the frequency of the DDS9m to 10MHz. Connect the DDS9m to the oscilloscope set for 50Ω termination. Set the oscilloscope to measure to amplitude using at least 16 averages. Verify a reading of 1Vpp $\pm 0.25\text{Vpp}$. Repeat for the other outputs.

6.5 Level Command Test. Leave the output frequency set to 10MHz. Send the commands “Vn 512” to each channel, where ‘n’ is your selected channel number. Verify that the amplitude on each channel decreases by one-half. Send the “R” command to reset the levels before performing the next tests.

6.6 Output Flatness Verification. Verify that the outputs are flat with frequency by performing the following test: Connect the DDS9m to the oscilloscope set for 50Ω termination. Set the output frequency to 35MHz. Note the voltage reading.

6.7 Set the DDS9m to the values shown in the Frequency Test Point list. Verify that the oscilloscope amplitude reading remains within $\pm 3\text{dB}$ (1.414 to 0.707) of the value noted in the previous paragraph.

6.8 Repeat the output flatness verification test for each output.

6.9 External Clock Input Verification. Set the frequency output to 10.000MHz by sending the command “F0 10.7374182” (scaled per section 4.0). Connect a 400MHz external clock source via a short coaxial cable to the external clock MCX. Send the command “Kp 01”. Send the command “C e” to select the external clock input.

6.10 Verify an output of 10.0000000MHz, $\pm 0.1\text{Hz}$. You must account for any frequency errors in your external clock source.

6.11 Return the DDS9m to normal operation and default values by sending the “CLR” command.

6.12 This concludes the verification test of the DDS9m

7.0 Calibration

7.1 The full scale output amplitude is adjustable using the ZCal0 x command. Where x is an integer from 0 to 127. x = 0 sets the output to the maximum value, x = 127 sets the output to the minimum value. Send ZCal9 to save the setting. ZCal0 = 127 is the factory default. No other calibrations are available.

8.0 Appendix A. Table Mode Details.

8.1 The Model DDS9m contains on-board memory capable of storing up to 32,768 profile points. Each point contains phase, frequency, amplitude and dwell time information. The on-board microcomputer reads this memory and programs the DDS ASIC per the profile point data. The profile can be set to loop continuously or to hold at the last point, until interrupted by a subsequent command.

NOTE:

Only Channels 0 and 1 can be set with the table mode.

8.2 The table mode is toggled on and off by an ‘M t’ command from the serial port and executes customer provided profile points. ‘M 0’ always turns off the table and returns to single tone mode. The DDS9m starts execution of the profile immediately upon a receipt of ‘M t’ following an ‘M 0’.

8.3 The command sequence (bold) is of this form (comments after the ‘;’ are not sent to the DDS9m, but are here for explanation purposes):

M 0

;turns off running table mode

t0 0000 aabbccdd,eeff,gghh,ii

;F0 profile point 0, on output 0

t1 0000 aabbccdd,eeff,gghh,ii

;F1 profile point 0, on output 1

t0 0001 aabbccdd,eeff,gghh,ii

;F0 profile point 1

t1 0001 aabbccdd,eeff,gghh,ii

;F1 profile point 1 ...

t0 3fff aabbccdd,eeff,gghh,ii

;F0 profile point 0x3fff

t1 3fff aabbccdd,eeff,gghh,ii

;F1 profile point 0x3fff

M t

;begin execution of table

;'0000' two byte memory address, T0 and T1 must be paired with same address

;'aabbccdd' four bytes frequency, hexadecimal, MSB first, 4 bytes. 0.1Hz resolution on LSB

;'eeff' phase offset, hexadecimal, MSB first, only 14-bits active, top two bits are ignored

;'gghh' amplitude scale, MSB first, only 10-bits active. Amplitude is scaled per above.

;'ii' dwell time, MSB first, in increments of 100µs. 0x00=loop back to start, 0xff=hold present setting. Each T0-T1 pair must have the same dwell.

8.4 The ‘,’ (comma) in each record is used as a delimiter and must be included as shown. The inputs are not case sensitive. Subsequent ‘M t’ commands will toggle the execution of the table on and off. Upon execution of the table, the output will always begin with address 0000 and progress until it encounters an 0xff or 0x00 in a dwell position. The last record in a table mode will be executed for 100µs if the dwell is set to 00.

NOTE:

Each record must be terminated with an 0x00 or 0xff in the dwell position to indicate the end of your data.

8.5 The current values stored in the table can be read back by the “Dn aaaa” command. N=0 or 1 and “aaaa” is the memory address.

Table 1: Serial Commands (Not Case Sensitive)

RS232 Command	Function
F n xxx.xxxxxxx	Set Frequency of output “n” in MHz to nearest 0.1Hz. n=0, 1, 2, 3. Decimal point required. 0.00 sets a channel to DC. Maximum setting: 171.1276031 MHz. Single tone mode.
P n N	Set Phase of output “n”. N is an integer from 0 to 16383. Phase is set to $N*360^\circ/16384$ or $N*\pi/8192$ radians. Sets the relative phase of the frequency output depending upon the value of n=0, 1, 2, 3. Single tone mode.
E x	Serial echo control. x=D for Echo Disable, x=E for Echo Enable
C x	Select clock source. x=E for External clock, x=I for Internal Clock. May require adjustment of Kp and external filtering of output. (Do not use this command if the /R option is installed.) x=D for a direct input clock where Kp = 1.
R	Reset. This command resets the DDS9m. Memory data is preserved and, if valid, is used upon restart. This is the same as cycling power.
CLR	Clear. This command clears the Memory valid flag and restores all factory default values.
S	Saves current state into memory and sets valid flag. State used as default upon next power up or reset. Use the “CLR” command to return to default values.
Q or Que	Returns DDS9m internal settings. (Que returns settings in Hex and is backwards compatible with earlier firmware versions)
M N	Mode command. N= 0 puts the DDS9m into single tone on all channels (default). N=t puts the DDS9m into Table Mode for channels 0 and 1. N=a and N=n control when the phase register is cleared (see paragraph 4.12)
V n N	Set voltage level of output. In default, the amplitude is set to the maximum: approximately 1Vpp (+4dBm) into 50Ω. N can range from 0 (off) to 1023 (no decimal point allowed). Voltage level is scaled by N/1023. n=0, 1, 2, 3 to set the amplitude on frequency 0, 1, 2 or 3. If N >=1024, the scaling is turned off and the selected output is set to full scale.
V s N	Set the output amplitude scaling factor. N=1 for full scale, N=2 for one half scale, N=4 for one quarter scale and N=8 for one eighth scale. All channels are scaled equally.
K p aa	Set PLL reference multiplier constant. Must be one Hexadecimal byte as two characters. Legal values are 1 (bypass PLL) and 4 to 20 (01, 04 to 14). Values of Kp times clock frequency must not be between 160 MHz and 255 MHz (for internal clock, this disallows $5 \leq Kp \leq 9$).
TS	Table Step command. If the M t command is set, TS causes the DDS9m to step through the table. Requires all dwell settings to be “ff”. The TS command can also be executed by a negative edge on the TS control input, pin 10 of connector P1.
D n aaaa	Read table values. n = output channel 0 or 1. aaaa = table address.
I x	Set the I/O update pulse method. If x=a, then an I/O update is issued at the end of each serial command (default). If x=m, then a manual I/O update pulse is sent by a subsequent ‘I p’ command. If x=e then I/O update is issued when a positive 3.3V edge is applied to the IOUD control input, pin 14 on connector P1.
B aa[bb[cc[dd[ee[ff[gg]]]]]]	This Byte command allows each register in the DDS chip to be set. Different registers require a various number of bytes to be written depending upon the function. Please consult Analog Devices AD9959 data sheet for details. Note that it is possible to set the DDS chip into a non-functional mode, requiring a power cycle to recover. All values are in hexadecimal and no error checking, other than correct format, is performed.

WARRANTY

NOVATECH INSTRUMENTS warrants that all instruments it manufactures are free from defects in material and workmanship and agrees to replace or repair any instrument found defective during a period of one year from date of shipment to original purchaser.

This warranty is limited to replacing or repairing defective instruments that have been returned by purchaser, at the purchaser's expense, to NOVATECH INSTRUMENTS and that have not been subjected to misuse, neglect, improper installation, repair alteration or accident. NOVATECH INSTRUMENTS shall have the sole right to final determination regarding the existence and cause of a defect.

This warranty is in lieu of any other warranty, either expressed or implied, including but not limited to any warranty of merchantability or fitness for a particular purpose. In no event shall seller be liable for collateral or consequential damages. Some states do not allow limitations or exclusion of consequential damages so this limitation may not apply to you.

All instruments manufactured by NOVATECH INSTRUMENTS should be inspected as soon as they are received by the purchaser. If an instrument is damaged in shipment the purchaser should immediately file a claim with the transportation company. Any instrument returned to NOVATECH INSTRUMENTS should be shipped in its original shipping container or other rigid container and supported with adequate shock absorbing material.

This warranty constitutes the full understanding between NOVATECH INSTRUMENTS and the purchaser and no agreement extending or modifying it will be binding on NOVATECH INSTRUMENTS unless made in writing and signed by an authorized official of NOVATECH INSTRUMENTS.

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