

NOVATECH INSTRUMENTS

INSTRUCTION MANUAL

Model 409B, 171 MHz, 4-Channel Signal Generator



Model 409B

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NOTE:

This Manual applies to 409B units with Firmware v2.1 or later.

1.0 DESCRIPTION

1.1 The Model 409B is a four-channel Direct Digital Synthesized (DDS) Signal Generator in a small table top case with serial control. The 409B provides four independent, phase-synchronous sine wave output signals, which can be set from 0.0 Hz (DC) to 171 MHz in 0.1 Hz steps when using the internal VCTCXO clock. (Consult factory if LVCMOS signals are desired.)

1.2 The 409B can also be used with an external clock input. An on-board programmable frequency multiplier generates the system clock allowing user configured frequency ranges. The multiplier can be disabled for direct inputs up to 500 MHz for optimum phase noise performance. When used with the same external clock source, multiple 409B are phase synchronous.

1.3 A Table Mode feature enables users to store frequency, phase, amplitude and dwell time settings in static RAM. The 409B can then run through the table automatically, step through it on command from the serial port or from an external hardware trigger.

1.4 The /R option converts the External Clock input to a 10.00 MHz reference input. This option allows locking to and tracking an external 10.00 MHz reference, with no binary round-off errors. When this option is installed the accuracy and stability of the output are equal to those of the reference.

1.5 The -AC option adds two SMA connectors on the rear panel and enables synchronization of frequency, phase and amplitude updates with external devices using user provided hardware trigger signals.

1.6 The /W option is no longer available.

2.0 SPECIFICATIONS

2.1 OUTPUTS

TYPES: Four sine waves simultaneously (four independent, phase-synchronous outputs).

IMPEDANCE: Sine: 50Ω; LVCMOS: 50Ω.

RANGE: 0.0 Hz to 171 MHz in 0.1 Hz steps (Sine out, int. clock).

SINE AMPLITUDE: approximately 1V_{pp} (+4dBm) into 50Ω. Programmable from 0/1024 to 1023/1024 of Full Scale (10-bits), or by scale factors of 1/2, 1/4, or 1/8.

PHASE: Each channel 14-bits programmable (0.022°).

FLATNESS: ±3dB from 1 kHz to 150 MHz referenced to amplitude at 35 MHz, full scale.

2.2 LVCMOS

V_{oh} ≥2.4V and V_{ol} ≤0.4V when series terminated.

Rise and fall times <1.5ns (>1 MHz, <125 MHz). Applies for LVCMOS Signal Outputs. Also applies for Option -AC IOUD and TS Trigger Inputs and Outputs.

(Consult factory for LVCMOS Signal Outputs)

2.3 CONTROL

Output frequencies, amplitudes (10-bits) and phases (14-bits) are controlled by a text commands sent to the 409B via a serial port at 19.2kbaud. All settings can be saved in non-volatile memory.

2.4 ACCURACY AND STABILITY

Accuracy: <±1.5ppm at 10 to 40°C. Stable to an additional ±1ppm per year, 18 to 28°C. (Internal Clock)

2.5 EXTERNAL CLOCK IN

LEVEL: 0.2 to 0.5 V_{rms} sine or square wave. 50Ω.

FREQUENCY: 10 MHz to 125 MHz with multiplier of 4 to 20 enabled. The external clock input times the K_p aa parameter cannot be between 160 and 255MHz. A direct input ("K_p aa" = 1) can be from 1 MHz to 500 MHz.

2.6 EXTERNAL REFERENCE (/R OPTION): External Reference must be 10.00 MHz, ±5ppm. Automatically detected. Internal clock is locked to and tracks this value.

2.7 SPECTRAL PURITY (Typical)

(50Ω load, internal clock, full-scale output)

Phase Noise: <-120dBc, 10 kHz offset, 10 MHz out.

Spurious:

<-60dBc below 10 MHz (typ. 300MHz span)

<-60dBc below 40 MHz

<-55dBc below 80 MHz

<-50dBc below 160 MHz

Harmonic:

<-65dBc below 1 MHz

<-55dBc below 20 MHz

<-45dBc below 80 MHz

<-35dBc below 160 MHz

(channel-channel isolation: <-60dBc)

2.8 TABLE MODE

On-board flash memory holds up to 14,250 rows of settings for each of two output channels, allowing new output values to be set every 100μs.

2.9 POWER REQUIREMENTS

+4.5 to +5.5 VDC <1Amp. AC adapter provided.

2.10 SIZE

39mm H, 107mm W, 172mm L, not including connectors.

2.11 CONNECTORS

BNC for Sine Outputs and EXT CLK IN. DE9 for Serial Control. 2.5mm center positive power receptacle for +5 volts input. AC Power adapter provided.

2.12 OPTIONS

OPTION /USB: Adds USB 2.0 Type B female connector and J8 connector. J8 pin numbers from left to right when facing the rear panel are 13,11,9,7,3,1 (top) and 14,12,10,8,6,4 and 2 (bottom). +IOUD is on pin 1, +TS is on pin3. All other pins are connected to instrument ground. Replaces DE9 RS232 connector.

OPTION /R: Phase locks the internal VCTCXO oscillator to an external 10MHz, customer supplied input.

OPTION -AC: Adds two SMA connectors on the 409B rear panel for IOUD and TS 3.3Vdc logic signals. A rising edge on these pins triggers updates that can be synchronized with external events;

3.0 HARDWARE INSTALLATION

3.1 Power Connection. The required power of +5Volts DC is applied through a 2.5mm center-positive power connector. The supplied AC power adapter comes with the correct mating connector.

WARNING:

Use of an unregulated source may damage the 409B. Use only the provided AC-adapter or consult Novatech Instruments for application assistance if you wish to use another power source.

3.2 Power Supply. The power supply should be free of ripple and noise (<100mV). Even though extensive filtering is used internal to the 409B, a quiet and well regulated power supply will ensure optimum performance.

3.3 USB Serial Interface Installation. The /USB option for the 409B requires the host computer to have a virtual COM port driver that is compatible with the 409B/USB port. This driver is made by Silicon Labs and is already installed on many computers. The driver can be found at:

<https://www.silabs.com/developers/usb-touart-bridge-vcp-drivers>.

The Silicon Labs VCPdriver for Microsoft windows is included on the USB memory stick that comes with the 409B. To install this driver from the memory stick, select the CP210xVCP Installer... application that matches the host computer and run it.

After installing the USB driver, connect the provided six foot USB cable to the 409C and the host computer.

3.4 RS232 Serial Interface Installation. If the 409B has a DE9 RS232 connector, then connect the provided 9-pin serial cable to the 409B DE9 connector. Host computers with nine pin RS232 ports can use this cable directly. If the host computer has a USB port but not an RS232 port then attach the provided FTDI XCHIP-X USB to RS232 Converter Cable to the 9-pin serial cable and then plug the Converter Cable into a USB port on the host computer.

A virtual COM port adapter or the XCHIP-X is already installed on many computers. If it is not already installed

it can be downloaded at:

<https://ftdichip.com/drivers/vcp-drivers/>

3.5 RS232 DE9 Connector Pinouts. The data **TO** the 409B is on pin 3; the data **FROM** the 409B is on pin 2 and the **COMMON** return is on pin 5.

3.6 Virtual COM Port Settings. The USB and RS232 virtual COM port settings should be set to match the 409B serial communication settings. These are 19.2 kBaud, 8 bits, 1 stop bit, no parity and no hardware flow control.

NOTE:

*The **SOF8_409 Software Program** is supplied on a USB Flash Drive with the 409B. This program has a COM port menu where you can view the available COM ports and select the COM port that is connected to the 409B. This software will automatically set the selected COM port to the 409C default COM Port settings. It also provides a graphical interface, enabling simplified control of the 409B.*

3.7 Serial Commands. Commands are not case sensitive. There must be a space after each command except R, CLR, S and QUE commands. Commands must end with any combination of Carriage Return (CR), Line Feed (LF) or CRLF. Illegal commands will result in an error code being returned per Table 1. Table 3 on the next page lists the serial commands.

Table 1: Error Codes

Error Code	Meaning
OK	Good Command Received
?0	Unrecognized Command
?1	Bad Frequency
?4	Bad Phase
?5	Bad Time
?6	Invalid Parameter
?7	Invalid Amplitude
?8	Invalid Baud Rate
?R	Table is Running
?S	Sweep must be disabled

Table 2. QUE Command Response Example

05F5E100 0000 03FF 0000 00000000 00000000 000301
05F5E100 1000 03FF 0000 00000000 00000000 000301
05F5E100 0000 03FF 0000 00000000 00000000 000301
05F5E100 1000 03FF 0000 00000000 00000000 000301
80 BC0000 0000 6102 21
<p>Description (All values above are in hexadecimal):</p> <p>The lines above describe current settings for the four output channel numbers 0,1,2 and 3 in sequence.</p> <p>For example, Channel 0 values are:</p> <p>“05F5E100” = frequency in 0.1Hz steps per LSB (10MHz);</p> <p>“0000” = phase setting (0);</p> <p>“03FF” = amplitude setting(1023).</p> <p>The last four groups of hex values on the first four lines and the entire last line describe AD9959 and microcontroller register settings for use by the factory.</p>

3.8 Query Commands. The ‘QUE’ command returns five hexadecimal strings reflecting the present state of the 409B. See Table 2 for an explanation of the values that make up these strings. The ‘Q’ command returns the values of settings in plain text and displays the firmware version.

3.9 Internal Clock. The 409B master clock is an internal TCXO crystal oscillator. If the 409B has option /R installed then the master clock is an internal VCTCXO oscillator that can be disciplined by an external 10MHz signal. The “C i” command selects the internal TCXO oscillator on the 409B or the internal VCTCXO oscillator on a 409B with option /R. The “C r” command activates the circuit that disciplines the internal VCTCXO oscillator on a 409B with option /R.

Table 3: Serial Commands (Not Case Sensitive)

RS232 Command	Function
Fn xxx.xxxxxxx	Set Frequency of output “n” in MHz to nearest 0.1Hz. n=0, 1, 2, 3. Decimal point required. 0.00 sets a channel to DC. Maximum setting: 171.1276031 MHz. Single tone mode.
Pn N	Set Phase. N is an integer from 0 to 16383. Phase is set to $N*360^{\circ}/16384$ or $N*\pi/8192$ radians. Sets the relative phase of the frequency output depending upon the value of n=0, 1, 2, 3. Single tone mode.
E x	Serial echo control. x=D for Echo Disable, x=E for Echo Enable
C x	Select clock source. x=i for Internal Clock, x=R for External 10MHz clock, x=E for External clock.
R	Reset. This command resets the 409B. Flash data is preserved and, if valid, is used upon restart. This is the same as cycling power.
CLR	Clear. This command clears restores all factory default values.
S	Saves current state into flash memory and sets valid flag. State used as default upon next power up or reset. Use the “CLR” command to return to default values.
QUE or Q	‘Que’ returns HEX values of frequency, phase and amplitude. ‘Q’ returns non-volatile settings in text.
M N	Mode command. N= 0 puts the 409B into single tone on all channels (default). N=t puts the 409B into Table Mode for channels 0 and 1. N=a and N=n control when the phase register is cleared (see paragraph 4.12). N=s Performs a manual reset on all channels.
Vn N	Set voltage level of output. In default, the amplitude is set to the maximum: approximately 1Vpp (+4dBm) into 50Ω. N can range from 0 (off) to 1023 (no decimal point allowed). Voltage level is scaled by N/1023. n=0, 1, 2, 3 to set the amplitude on frequency 0, 1, 2 or 3. If N >=1024, the scaling is turned off and the selected output is set to full scale. Sweep must be disabled to set voltage level.
Vs N	Set the output amplitude scaling factor. N=1 for full scale, N=2 for one half scale, N=4 for one quarter scale and N=8 for one eighth scale. All channels are scaled equally.
Kp aa	Set PLL reference (clock) multiplier constant. Must be one Hexadecimal byte as two characters. Legal values are 01, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13 or 14 (this is 1 (bypass PLL) and 4 to 20 in decimal). Values of Kp times clock frequency must not be between 160 MHz and 255 MHz.
TS	Table Step command. If the M t command is set, TS causes the 409B to step through the table. Requires all dwell settings to be “ff”. The TS command can also be executed by a negative edge on the rear mounted TS control input. (Option -AC adds the TS control input.)
Dn aaaa	Read table values. n = output channel 0 or 1. aaaa = table address.
I x	Set the I/O update pulse method. If x=a, then an I/O update is issued at the end of each serial command (default). If x=m, then a manual I/O update pulse is sent by a subsequent ‘I p’ command. If x=e then I/O update is issued when a positive 3.3V edge is applied to the rear IOUD control input. (Option -AC adds IOUD control input.)
B a a[b b[c c[d d[e e[f f[g g]]]]]]	This Byte command allows each register in the DDS chip to be set. Different registers require various number of bytes to be written depending upon the function. Please consult Analog Devices AD9959 data sheet for details. Note that it is possible to set the DDS chip into a non-functional mode, requiring a power cycle to recover. All values are in hexadecimal and no error checking, other than correct format, is performed. Each byte to be one or two hex digits, separated by a space, tab or comma.

3.10 External Clock. Sending the serial command ‘C e’ will configure a 409B or a 409B with option /R to use an externally provided signal as the master clock, bypassing the internal oscillator. This external frequency signal needs to be connected to the rear panel BNC connector. Note that phase noise and stability are dependent upon the user supplied external clock. See specifications in Section 2 for signal levels required and acceptable frequency range.

3.11 PLL Multiplier. A phase lock loop (PLL) multiplier in the AD9959 DDS IC steps up the master clock and this stepped up frequency is used as the synthesizer clock frequency. Sending the command ‘Kp aa’, where aa must be the number 1 or 4 to 20, selects the PLL multiplier.

NOTE

The value of Kp times the master clock frequency must not be between 160MHz and 255MHz.

The synthesizer clock frequency is then equal to the master clock frequency times the PLL multiplier. When using the internal clock, KP aa is set to 15 by the internal micro controller. Setting Kp=1 disables the PLL multiplier. This enables the use of a direct input up to 500 MHz, for optimum phase noise performance.

CAUTION:

If the synthesizer clock frequency exceeds 500 MHz, you may overheat and damage the 409B.

NOTE:

When using an external clock, scaling of the “Fn” command will most likely be required. Please see Operation, Section 4, for details.

3.12 Signal Outputs. There are four signal outputs on the 409B labeled 0 to 3 on the front panel. These correspond to frequency (F0 through F3), phase (P0 through P3), and voltage (V0 to V3) commands. Simply connect your 50Ω application cable to the appropriate output BNC connector.

3.13 Rack Mounting. An optional 1U rack adapter is available for mounting up to four 409B into a rack panel. Please consult factory.

4.0 OPERATING INSTRUCTIONS

4.1 Power on reset. After power is applied, the 409B takes approximately 500ms to initialize. Commands sent during this time will be ignored or may cause erroneous operation.

4.2 Warmup. Specifications are met within approximately 15 minutes of power up.

4.3 Commands. After the 409B has been installed in the customer application system, all that is required for operation is to send the appropriate serial commands as shown in Table 3 on page 5 and table 3S on page 10.

NOTE

The “B” command shown in Table 3 can be used to test the AD9959 DDS chip programming as it allows access to all internal registers. While not a real-time simulation, each “B” command functions as an input by putting a data byte directly into the AD9959 via an SPI port, and then pulses the IOUD line. This is similar to a procedure that a customer control circuit might perform. The “B” command values are not saved so they will not show in the Q or QUE command output. Consult the Analog Devices for support. Novatech Instruments does not provide tech support for the “B” command

4.4 Error Codes. The user host computer software must properly format the serial commands. Incorrect formatting will result in an error code being returned. See Table 1 in section 3 for a list of error codes.

4.5 Echo. For maximum interface speed, it is suggested that Echoing be disabled by using the “E d” command. This will allow the host to send characters at a faster rate. Even when Echo is disabled, the 409B will respond with an “OK” for a correctly received data command.

4.6 Baud Rate. A special command, “Kb n”, is available if you wish to set a baud rate that is different from the default of 19.2KBaud. The value set by this command is volatile. Upon power up the 409B defaults to 19.2kBaud. The available “Kb n” commands are:

- Kb 0 (Set to 9.6kBaud)
- Kb 1 (Set to 19.2KBaud)
- Kb 2 (Set to 38.4KBaud)
- Kb 3 (Set to 57.6KBaud)
- Kb 4 (Set to 115.2KBaud)

4.7 External Clock & Frequency Scaling. When using the 409B default settings, the frequency command is the same as the desired output frequency. However, when using an external clock, the frequency command will likely not be the same as the desired output frequency. The calculation needed to determine the frequency command when using an external clock is as follows:

$$(F_{\text{command}}) = (F_{\text{out}}) (429.4967296\text{MHz}) / (K_p * F_{\text{ext clk}})$$

Where:

F_{command} = The frequency command in MHz.

F_{out} = The desired 409B output frequency in MHz.

K_p = value of clock multiplier

$F_{\text{ext clk}}$ = the external clock input frequency in MHz.

NOTE:

Scaling is not required when option /R is installed and in use.

4.8 Example of Frequency Scaling. For an example of scaling, suppose an external clock of 10.000 MHz and K_p of 15 is used and an output of 1.544 MHz is desired. Then ($K_p * F_{\text{ext clk}}$) = 150MHz and the command is:

$$(F_{\text{command}}) = (1.544\text{MHz}) (429.4967296\text{MHz}) / (150\text{MHz})$$

$$(F_{\text{command}}) = 4.4209530$$

To set output channel 0 to 1.544 MHz, send the command “F0 4.4209530”. There should also be an external filter at 60MHz (40% of 150MHz) or less or there will be excessive distortion on the output signal.

4.9 External Clock and Filters. When using an external clock, best performance is obtained by setting K_p such that the value K_p times the external clock frequency is as close as possible to 500MHz. The 409B on-board low pass filters are optimized for synthesizer clock frequencies of 429MHz or higher. If the external clock frequency times the clock multiplier (K_p) is significantly lower than 429MHz, then external filtering may be needed to prevent output signal distortion. It is recommended that the external filters have roll off frequencies that are equal to or below 40% of the external clock frequency times K_p .

4.10 Range Bit. It is possible to control the internal range bit on the AD9959 DDS ASIC using the K_p command. For applications using the internal oscillator the K_p command is unmodified. However, it may be desirable that the clock multiplier gain bit be set HIGH (for external clocks where the system clock ($K_p \times$ External Clock Frequency) is from 255 to 500 MHz). To do this add hexadecimal 80 to the K_p value to be set. For the bit to be forced LOW (for external clocks where the system clock is 100 to 160 MHz), add hexadecimal 40 to the K_p value to be set.

4.11 Fractional Frequency Errors. When using the default system clock or an external clock there may be a small calculation round off error. The round off error as a fractional frequency error ($\Delta f/f$) for output frequencies in the MHz range will be less than 0.1ppm.

NOTE:

When using a 10 MHz external reference with Option /R installed, there is no fractional frequency error.

4.12 Phase Alignment. Phase relationships are maintained by appropriate use of the “M” and “I” commands. The “M” command has special modes “M a” and “M n”. “M a” means automatically clear phase at the end of each command. This will clear the phase register each time any command is performed. This is important when all outputs must be phase aligned. However, it will cause a phase jump in the output.

4.13 Phase Synchronous. The “M n” command turns off the automatic clearing of the phase register. This is the default mode. In this mode, the phase register is left intact when a command is performed. Use this mode if you want frequency changes to remain phase synchronous, with no phase discontinuities.

4.14 Command Execution. Further control of phase relationships and timing of command execution can be exercised by using the “I a”, “I m”, “I p” and “I e” commands. The default mode is “I a” in which a command is parsed and executed immediately following the end of the serial input sequence. In the “I m” mode, an update pulse will not be sent to the DDS chip until an “I p” command is sent. This is useful when it is important to change all the outputs to new values simultaneously. The “I e” command is used with the –AC Option.

4.15 Amplitude Matching. For applications which require precise amplitude matching between the channels, the recommended method is to use the “Vn N” command to adjust the channels to match. This command provides 10-bits of adjustment range.

4.16 Table Mode. The Model 409B contains on-board non-volatile memory capable of storing up to 14,250 table row combinations. A combination consists of the settings for each of two output channels. Each row contains phase, frequency, amplitude and dwell time information. The on-board microcomputer reads each row and programs the AD9959 DDS ASIC with the row settings.

NOTE:

Only Channels 0 and 1 generate outputs when using the table mode.

4.17 Running a Table. An ‘m 0’ command always turns off the table mode and returns the 409B to single tone mode. If the 409B is in single tone mode, sending an “m t” command to the 409B will put it into the table mode and cause the 409B to start running the settings stored in the table rows. Sending more “m t” commands will toggle the table mode on and off.

4.18 Loading the Table. The command sequence to load row data into the table is of the following form:

```
m 0
t0 0000 aabbccdd,eeff,gghh,ii
t1 0000 aabbccdd,eeff,gghh,ii
t0 0001 aabbccdd,eeff,gghh,ii
t1 0001 aabbccdd,eeff,gghh,ii
.. etc
m t
```

Where:

m 0 puts the 409B into single tone mode.
t0 and **t1** mean load row data for output 0 and 1
0000 is a two byte hex address, **t0** and **t1** must be paired with the same address.
aabbccdd is a four byte hex frequency setting, MSB first, 0.1 Hz resolution on LSB
eeff is a hex phase offset setting, MSB first, only 14-bits active
gghh is a hex amplitude setting, MSB first, only 10-bits active.

ii is dwell time, MSB first, in increments of 100µs. “00” means loop back to start, “ff” means hold present setting. **m t** puts 409B into table mode and runs the table.

4.19 Table Formatting. Each **t0** and **t1** pair must have the same dwell setting. The “,”(comma) in each record is used as a delimiter and must be included as shown. The inputs are not case sensitive. Subsequent “m t” commands will toggle the execution of the table on and off. Upon execution of the table, the output will always begin with address “0000” and progress until it encounters an “ff” or “00” in a dwell position. The last record in a table will be executed for 100µs if the dwell is set to “00”.

4.20 Single Stepping the Table. In single step operation the 409B makes use of dwell times (**ii**) set to “ff”. The data in each **t0** and **t1** pair with a dwell time of “ff” can be stepped to the next setting by sending a TS serial command or by hardware triggering using the rear mounted TS connector (Option –AC required for hardware triggering).

4.21 Looping and Pausing the Table. If the dwell setting (**ii**) in a **t0** and **t1** pair are set to “00” then the table will loop back to start. If these dwell settings are set to “ff” then the table will hold the present settings unless/ until the 409B receives a TS command or TS hardware trigger.

NOTE:

The last row pair in the table must be terminated with an “00” or “ff” in the dwell position.

4.22 Stop Running a Table. Sending an “m 0” command will stop the 409B from running the table.

4.23 Example Table for Single Stepping. This example starts with both output channels having 10MHz frequency, zero phase, and full scale amplitude then steps to 5MHz, zero phase, half scale amplitude and then repeats.

```

m 0
t0 0000 05f5e100,0000,03ff,ff
t1 0000 05f5e100,0000,03ff,ff
t0 0001 02faf080,0000,0200,ff
t1 0001 02faf080,0000,0200,ff
t0 0002 02faf080,0000,0200,00
t1 0002 02faf080,0000,0200,00
m t
ts
ts

```

“m t “ starts the table and runs the first set of “t0” and “t1” rows.

“ts” steps to the second set of “t0” and “t1” rows.

“ts” steps to the last set of “t0” and “t1” rows where the “00” in dwell causes the profile to run for 100 microseconds and then loop back to the start.

NOTE:

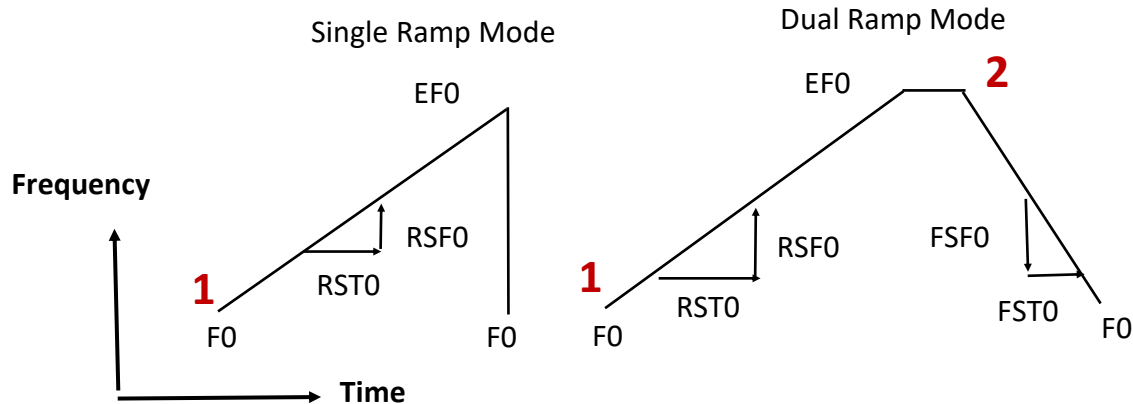
The included SOF8_409 software provides menu tools to load the table. It also uses decimal numbers instead of hex numbers. The decimal numbers are automatically converted to hex and then sent to the 409B.

4.24 Table Synchronization with External Events.

For precision timing application it is recommended that external table synchronization be used. This involves triggering table operations using customer supplied external hardware. Option -AC is required for external table synchronization. See Section 9 for detailed instructions.

4.25 Reading Table Values. The current values stored in the Table can be read by sending the “Dn aaaa” command where “n” is 0 (“t0”) or 1 (“t1”) and “aaaa” is the table address.

FREQUENCY SWEEP MODES



SINGLE SWEEP MODE CHANNEL 0

DUAL SWEEP MODE CHANNEL 0

Point 1 shows the Trigger point to start the sweep

F0 Beginning & Ending Frequency

RST0 Rising Step Time

RSF0 Rising Step Frequency

EF0 End of Rising Frequency

NOTE:

Sweep commands start with SW. Thus, to set the rising step time of channel 0 to 1 microsecond the command would be **SWRST0 1**

Point 1 shows the Trigger point to start the rising sweep

Point 2 shows the trigger point to start the falling sweep

F0 Beginning & Ending Frequency

RST0 Rising Step Time

RSF0 Rising Step Frequency

EF0 End of Rising Frequency

FSF0 Falling Step Time

FST0 Falling Step Frequency Channel 0

4.26 Frequency Sweeping. 409B Models with serial numbers 24000 or higher have a sweep feature that enables the user to set a begin frequency and an end frequency for each output channel (n = 0,1,2,or 3) and then perform one of the following sweep modes:

- 1) Ramp up and Ramp down (set with command ‘SWMDn D’).
- 2) Ramp up and step down (set with command ‘SWMDn S’).

4.27 Set Up a Sweep. The beginning frequency is set using the ‘Fn xxx.xxxxxxx’ command. The ending frequency must be larger than the beginning frequency and is set using the ‘SWEFn xxx.xxxxxxx’ command.

The frequency step size is programmable when ramping up and also when ramping down . The ramp up frequency step size is set by the ‘SWRSFn xxx.xxxxxxx’ command and the ramp down frequency step size is set by the ‘SWFSFn xxx.xxxxxxx’ command.

The time duration of each step is programmable when

Table 3S: Serial Commands for Frequency Sweeping (Not Case Sensitive)

Command	Function
SWENBn x	Enable Sweeping. n = Output channel number, x = E for enable or x = D for disable
SWMDn x	Sweep Mode. n = Output channel number, x = S sets ramp up step down, x = D sets ramp up and ramp down.
SWEFn xxx.xxxxxxx	Ending Frequency. n = Output channel number, xxx.xxxxxxx = Ending frequency in MHz. (Beginning frequency is set by the Fn xxx.xxxxxxx command)
SWRSFn xxx.xxxxxxx	Rising Frequency Step Size. n = Output channel number, xxx.xxxxxxx = Frequency step size in MHz
SWFSFn xxx.xxxxxxx	Falling Frequency Step Size. n = Output channel number, xxx.xxxxxxx = Frequency step size in MHz
SWRSTn t	Rising Time Step Size. n = Output channel number, t = Step size in Microseconds
SWFSTn t	Falling Time Step Size. n = Output channel number, t = Step size in Microseconds
PPn x	Set Trigger Low/Hi. n = Output channel number, x =0 sets trigger Low or x = 1 sets trigger high.

Example of Single Sweep from 10MHz to 60MHz in 10 seconds on Channel 0

Send the following commands: f0 10, swef0 60, swrst0 2, swrsf0 0.00001, swenb0 e, swmd0 s.

Trigger a sweep from software by sending the following commands: pp0 0 then pp0 1.

NOTE: Sweep time is 50MHz/10Hz per step = 5,000,000 steps times 2 μS/step = 10 seconds.

Example of Dual Sweep from 10MHz to 60MHz to 10MHz on Channel 0

Send the following commands: f0 10, swef0 60, swrst0 2, swfst0 2, swrsf0 0.00001, swfsf0 0.00001, swenb0 e, swmd0 d.

Trigger a sweep in software by sending the following commands: pp0 0 then pp0 1 (starts rising sweep) then send pp0 0 (starts falling sweep).

ramping up and also when ramping down. The time duration when ramping up is set by the 'SWRSTn t' command and the time duration when ramping down is set by the 'SWFSTn t' command.

The parameter 't' above can be from 0.009 microseconds to 2.2 microseconds when using the internal clock or the /R option. When using an external reference clock or direct clock the parameter 't' has a minimum of 4/Fs and a maximum of 1020/Fs where Fs is the Synthesis Clock frequency that is displayed by sending the 'q' command.

NOTE:

Entering a step time t that is larger than the maximum allowed value for t will result in the step time being set to the maximum allowed value.

4.28 Total Sweep Time. To compute the total time a sweep will take, first compute the total number of steps. This is the begin frequency minus the end frequency divided by the frequency step size. The sweep time will then be the number of steps times the step time.

4.29 Running a Sweep. To execute a sweep the user must first enable sweeps using the 'SWENBN x' command where x can be E for enabled and D for disabled. Once enabled the sweep will start by setting the trigger to rise from 0 to 1 using the 'PPn x' command where x can be 1 or 0. Sending a 'PPn 0' followed by a 'PPn 1' causes a trigger rise.

4.30 Sweep Default Settings. The default sweep settings for output channel 0 are as follows:

F0=10.0000000 P0=0.00 V0=1.000
(Begin frequency = 10MHz, Phase = 0, Vout = 1Vpp)

SWEF0=150.0000000
(Ending frequency = 150MHz)

SWRSF0=1.0000000 SWFSF0=1.0000000
(Rising and falling frequency steps = 1 MHz)

SWRST0=1.000 SWFST0=1.000
(Rising and falling time steps = 1 microsecond)

SWMD0=S SWENB0=D
(Sweep mode set to Ramp up and Step down. Sweep Enable/Disable set to Disable)

4.30 Sending Sweep Commands. It is recommended that the SOF8_409 software command menu be used to set the sweep parameters and run the sweep. Sending a 'q' command will display the current settings of the sweep parameters on all output channels.

5.0 THEORY OF OPERATION

5.1 Block Diagram. Please refer to the simplified System Block Diagram in Figure 1 for the following discussion.

5.2 DDS. At every cycle of the 409B system clock, the AD9959 integrated circuit increments the phase of an internal register by a value calculated from the frequency command and sent to the AD9959 by the microcontroller. The AD9959 converts this phase value to a sinusoidal amplitude level and then sets the values of on-chip 10-bit digital-to-analog converters. The analog signals from these converters are filtered by differential 7th-order elliptical low pass filters, amplified and sent to the 409B output connectors.

5.3 Clock Multiplier. The AD9959 has an internal PLL clock multiplier that can be set with the Kp command to a value of 1 or a value from 4 to 20. When using an external clock, the synthesizer clock frequency is equal to the master clock frequency times the clock multiplier. Values of the synthesizer frequency between 160MHz to 255MHz and above 500MHz are not allowed.

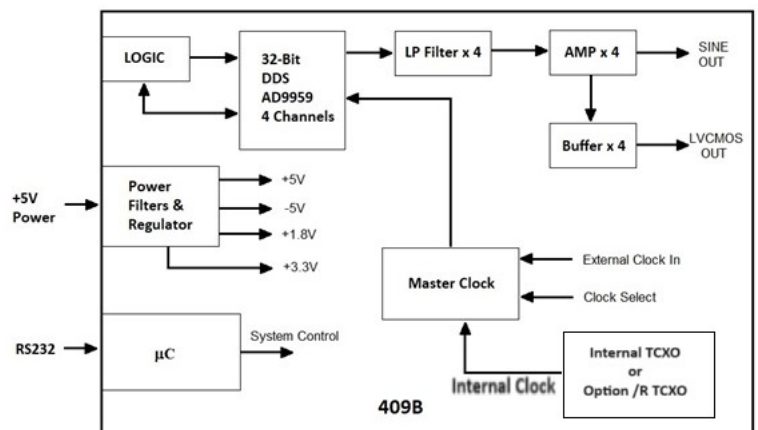


Figure 1
Simplified System Block Diagram

5.4 Frequency Calculation. When using the 409B internal clock the generated frequency is:

$$F_{out} = F_{command}$$

When using an external frequency as the 409B master clock the generated frequency is:

$$F_{out} = (F_{command} * Kp * F_{clock}) / 429.4967296$$

Where: F_{out} = 409B output frequency in MHz.
 $F_{command}$ = Commanded Frequency set with the Fn command where n is the channel number
 Kp = Clock Multiplier (1 or 4 to 20)
 F_{clock} = External clock frequency.

5.5 Maximum Frequency. The 409B theoretical output frequency is limited to a maximum of 1/2 the system clock frequency. While it is possible to generate an output near 50% of the system clock, the distortion would be unacceptable. The 409B frequency output is limited to 171MHz by 7th-order elliptical low pass analog filters on each of the four output channels.

5.6 External Filters. External filters are NOT needed when using the internal TCXO or the /R option TCXO as the master clock. However, if you are using an external clock where the synthesizer clock frequency (i.e the external clock frequency times Kp) is substantially lower than 429MHz, you may need external filters with lower cutoff frequencies to obtain acceptable results. For best performance, set the corner frequency at 40% or less of your synthesizer clock frequency.

5.7 External Filter Example. When using a 10 MHz external clock, with the default clock multiplier (Kp) of 15, the synthesizer clock will be 150 MHz. An optimal external filter for this frequency would then be approximately 60 MHz (40% of 150MHz).

NOTE

External filters are NOT needed when Option /R is installed and in use.

6.0 PERFORMANCE TEST

6.1 Setup. Install the 409B as directed in the Serial Operation part of Section 3. Connect your host controller and operate the 409B per Section 4. The test limits assume a stable environment of 18-28°C.

NOTE:

Allow the 409B to warm up for at least 15 minutes before performing any measurements. For best results, the 409B should be verified in its installed environment.

6.2 Test Equipment. See Table 4 on the next page for a list of recommended test equipment to perform the following measurements.

6.3 Verify Frequency Accuracy. To verify the frequency of the 409B, set the output sequentially to each value in Table 5. Connect the recommended frequency counter set to 50Ω termination and 1 Hz resolution. Verify the limits shown in Table 5. Test all channels to verify functionality of all outputs. If you do not use an external reference for the frequency counter, be sure to add the error of your counter to the tolerance. (LSD = Least Significant Digit on counter).

6.4 Sine Out Amplitude Verification. Set the frequency of the 409B to 10 MHz. Connect the 409B to the oscilloscope set for 50Ω termination. Set the oscilloscope to measure amplitude using at least 16 averages. Verify a reading of 1Vpp ±0.25Vpp. Repeat for the other outputs.

6.5 Amplitude Level Test. Leave the output frequency set to 10 MHz. Send the command “Vn 512” to each channel, where “n” is your channel number being tested. Verify that the amplitude on each channel decreases by one-half. Send the “R” command to reset the levels before performing the next tests.

6.6 Output Flatness Verification. Verify that the outputs are flat with frequency by performing the following test: Connect the 409B to the oscilloscope set for 50Ω termination. Use the same settings as Sine Out Amplitude Verification. Note the voltage reading.

6.7 Set the 409B to the values of Table 5. Verify that the oscilloscope amplitude reading remains within ±3dB (x1.414 to x0.707) of the value noted in the previous paragraph. (Limit upper frequency to 150 MHz.)

6.8 Repeat the output flatness verification test for each output.

6.9 External Clock Input Verification. Connect a 400 MHz external clock source via a short coaxial cable to the external clock input BNC on the rear panel. Send the command “Kp 01”. Send the command “C e” to select the external clock input. Set the frequency output to 10.000 MHz by sending the command “F0 10.7374182” (scaled per section 4.0).

6.10 Verify an output of 10.0000000 MHz, ± 15 Hz. You must account for any frequency errors in your external clock source.

6.11 Return the 409B to normal operation and default values by sending the “CLR” command.

6.12 This concludes the verification test of the 409B.

7.0 CALIBRATION

7.1 The full scale output amplitude is adjustable using the “ZCal0 x” command. Where x is an integer from 0 to 127. x = 0 sets the output to the maximum value, x = 127 sets the output to the minimum value. Send “ZCal9” to save the setting. “ZCal0 127” is the factory default. No other calibrations are available.

Table 4: Recommended Test Equipment

Item	Minimum Specification	Recommended
Oscilloscope	300 MHz 50 Ω	Tektronix TDS3032B
50 Termination	50 Ω $\pm 1\%$	Tektronix 011-0049-01 or HP53132A
Frequency Counter	180 MHz	HP53132A
Counter Time Base	10 MHz < ± 0.1 ppm	Novatech Instruments Model 2960AR
External Clock	400 MHz	Novatech Instruments Model 440A

Table 5: Frequency Test Points

Frequency	Tolerance
100 kHz	± 0.15 Hz ± 1 LSD
1 MHz	± 1.5 Hz ± 1 LSD
10 MHz	± 15 Hz ± 1 LSD
30 MHz	± 45 Hz ± 1 LSD
50 MHz	± 75 Hz ± 1 LSD
100 MHz	± 150 Hz ± 1 LSD
170 MHz	± 255 Hz ± 1 LSD

8.0 OPTION /R: LOCK TO 10MHz EXTERNAL INPUT

8.1 The /R option provides locking and tracking circuitry to phase lock the internal VCTCXO master oscillator to an external 10MHz reference.

8.2 A 10MHz reference must be connected to the rear panel BNC connector. See paragraph 2.5 for the required specs of this signal. The 10MHz input signal is automatically detected and, if within a lock range of approximately ± 5 ppm, it is locked to and tracked by a narrow-band phase lock loop.

8.3 If an input signal is not detected, the unit will default to using the VCTCXO master oscillator in free-running mode.

8.4 The front panel LED will display four conditions:

Steady Green: The 409B is locked to and is tracking a stable external 10 MHz signal.

Blinking Green: The 409B is trying to lock to an external 10 MHz Signal (fast blinking) or there is no external 10MHz input (slower blinking). When blinking green the 409B is using the free running VCTCXO master oscillator.

Steady Red: The 409B detects an external input, but cannot lock to it. The 409B is not using the free running VCTCXO oscillator and master the output frequency is in an unknown state.

8.5 When changing the reference mode, the phase lock loop may take several minutes to stabilize to the final resolution of the 409B. Changing from a blinking LED to a stable LED indicates that the process is completing, but you should verify the outputs.

9.0 OPTION –AC: EXTERNAL TIMING CONTROL.

9.1 Description. Option –AC adds two rear mounted SMA connectors, labeled IOUD and TS, that can be used for triggering and synchronizing 409B outputs.

9.2 IOUD Output vs Input. By default, the signal on the IOUD connector is an output indicating that the microcontroller has triggered an update to the 409B front panel sine wave outputs. Sending the “I e” command changes the IOUD from an output to an input and requires that an external trigger pulse be applied to the IOUD connector to update the 409B outputs.

NOTE:

If the IOUD is set as an input, running the table by sending an “M t” command will change it to an output. To make the IOUD an input when running the table, an “I e” command must be sent after the “M t” command is sent.

9.3 IOUD Used as Output. When the 409B microcontroller updates the 409B, it pulses IOUD high for about 150 nanoseconds. The actual trigger happens on the rising edge of this signal and this rising edge can be read by the users hardware.

9.4 Table Step (TS) Input. The TS connector is always an input when the table is running. It functions just like the “ts” serial command. If a table is running and is configured for single stepping, then applying a falling 3.3Vdc trigger signal to the TS connector will step through the table. An edge occurring sooner than about 100 μ s from the previous TS trigger will be ignored. Detection of the edge is affected by the current state of the microcontroller processing.

9.5 Microcontroller Triggering of the Table. This is the default process. The IOUD signal is set as an output. In response to an “m t” or “ts” serial command or to a TS connector trigger input, new settings are moved from table RAM into registers in the AD9959 DDS ASIC. This takes about 100 μ s. The microcontroller then puts a 150 nanosecond trigger pulse on the IOUD pin. The rising edge of this trigger causes the AD9959 DDS ASIC to update both table output channels within 100 \pm 8 nanoseconds.

9.6 Configuring IOUD as an Input. Sending an “I e” command will change the IOUD connector from an output to an input. Triggering the 409B to update the front panel outputs will then require a hardware trigger be applied to the IOUD connector. Sending an “M t” command to start running a table resets the IOUD to an output so the “I e” command must be sent after an “M t” command in order to use the IOUD connector as an input for triggering table updates.

9.7 Single Stepping a Table when IOUD is an Input. The AD9959 DDS ASIC must be preloaded with a new set of values about 100 μ s prior to applying an IOUD trigger. Preloading is done with the “ts” command or by applying a trigger signal to the TS connector. Once preloaded, the 409B can be triggered to update all outputs by applying a 3.3Vdc signal to the IOUD connector. The trigger will happen on the rising edge. The update to the outputs will have a pipeline delay of less than 100 nanoseconds \pm 8 nanoseconds from the positive edge of the IOUD trigger signal.

9.8 More Precise Timing with External Triggering. Using external triggering enables the user to take control of exactly when the outputs are updated. This avoids the uncertainty regarding the exact amount of time the processor will take to move data from RAM to the AD9959 DDS ASIC registers. While the user must still allow 100 μ s of time for this data to move from memory to the AD9959, the timing of the IOUD trigger update is decoupled from this time uncertainty. This method also enables the user to more easily synchronize updates with external events. External triggering can be used with the table mode and it can also be used sending serial commands to update the outputs.

9.9 Initialization Issue. Please note that the 409B needs to take control of the IOUD pin during 409B initialization. Initialization happens when power is applied to the 409B or after a reset command has been sent. For this reason, the user should not connect external signals to the IOUD connector during an initialization process.

WARRANTY

NOVATECH INSTRUMENTS warrants that all instruments it manufactures are free from defects in material and workmanship and agrees to replace or repair any instrument found defective during a period of one year from date of shipment to original purchaser.

This warranty is limited to replacing or repairing defective instruments that have been returned by purchaser, at the purchaser's expense, to NOVATECH INSTRUMENTS and that have not been subjected to misuse, neglect, improper installation, repair alteration or accident. NOVATECH INSTRUMENTS shall have the sole right to final determination regarding the existence and cause of a defect.

This warranty is in lieu of any other warranty, either expressed or implied, including but not limited to any warranty of merchantability or fitness for a particular purpose. In no event shall seller be liable for collateral or consequential damages. Some states do not allow limitations or exclusion of consequential damages so this limitation may not apply to you.

All instruments manufactured by NOVATECH INSTRUMENTS should be inspected as soon as they are received by the purchaser. If an instrument is damaged in shipment the purchaser should immediately file a claim with the transportation company. Any instrument returned to NOVATECH INSTRUMENTS should be shipped in its original shipping container or other rigid container and supported with adequate shock absorbing material.

This warranty constitutes the full understanding between NOVATECH INSTRUMENTS and the purchaser and no agreement extending or modifying it will be binding on NOVATECH INSTRUMENTS unless made in writing and signed by an authorized official of NOVATECH INSTRUMENTS.

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