NOVATECH
INSTRUMENTS

# 400MHz Programmable Signal Source

## Model 440A


The Model 440A Programmable Signal Source generates a low distortion sinewave signal from 200kHz to 400MHz with 1Hz resolution. The 440A contains an internal temperature compensated crystal oscillator that can be locked to an external reference in 8kHz steps, allowing the 440A to lock to common telecom signals, such as T1 and E1 rates, as well as common instrumentation frequencies such as 5MHz and 10MHz without external hardware. When locked, the accuracy and stability of the 440A will match that of the reference. The relative phase of the 440A can be controlled with 14-bits of resolution. The 440A is set by sending simple text commands over a 19.2kBaud serial interface. Four 440A can be mounted in a 1U rack and eight in a 2U rack with optional rack adapters. The 440A operates from a single +5VDC power supply (AC-line adapter provided).

## Specifications:

### OUTPUT

TYPE: Sine. (optional ECL/TTL)
IMPEDANCE: 50Ω.
RANGE: 200kHz to 400MHz in 1Hz steps.
AMPLITUDE: approximately 0dBm (630mV$_{pp}$ set at 10MHz) into 50Ω.

### CONTROL

Output frequency (32-bits) and phase (14-bits) are controlled by sending simple text commands over a bit-serial interface port (RS232) at 19.2kBaud. Settings can be saved in EEPROM via the serial port.

### ACCURACY AND STABILITY

Accuracy: <±1.5ppm at 10 to 40°C. Stable to an additional ±2ppm per year, 18 to 28°C. (Internal Clock)

### REFERENCE CLOCK IN

LEVEL: 0.5-3.0Vrms Sine or Square Wave. 50Ω.
FREQUENCY: Programmable from 1MHz to 25MHz, in 8kHz steps. The 440A will track the externally supplied reference as long as the external frequency is within ±5ppm. When locked the output frequency maintains the accuracy and the stability of the reference clock with no binary round-off. The external reference can be disabled to use the internal oscillator in free-run mode.

### SPECTRAL PURITY (Typ. 50Ω load, 10MHz ref.)

Phase Noise: <-120dBc, 10kHz offset, 10MHz output.

| | |
|---|---|
| Spurious: | <-55dBc below 10MHz (typ. 500MHz span) |
| | <-50dBc below 80MHz |
| | <-45dBc below 160MHz |
| | <-35dBc below 400MHz |
| Harmonic: | <-60dBc below 1MHz |
| | <-55dBc below 20MHz |
| | <-50dBc below 80MHz |
| | <-40dBc below 160MHz |
| | <-35dBc below 400MHz |

### POWER REQUIREMENTS

+5VDC (+4.75 to +5.25) @<1.0A. (90-240VAC with provided AC-adapter)

### SIZE

39mm H, 107mm W, 172mm L, not including connectors. Shielded aluminum case.

### ENVIRONMENTAL

Temperature: 0°C to +50°C operating.
Humidity: 80% to 31°C, decreasing linearly to 50% at 40°C.

### CONNECTORS

Sine: front panel SMA; Reference In: rear panel BNC. RS232 control: DE9F on rear panel. +5V DC Power: 2.5mm power receptacle, center positive.

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## Serial Commands

| RS232 Command | Function |
|---|---|
| F0 xxx.xxxxxx | Set Frequency Zero in MHz to nearest 1Hz. Decimal point required. Maximum 'F0' setting is 402.653183MHz |
| Fr xx.xxx | Sets the Reference Frequency in MHz in 8kHz steps. Decimal point required. Range: 1MHz to 25MHz. This value is used to phase lock the internal master clock to the externally supplied clock. Software rounds down to lowest 8kHz multiple. |
| P0 N | Set Phase Zero. N is an integer from 0 to 16383. Phase is set to N*360/16384 degrees (N*π/8192 radians). This command sets the relative phase of the output sine wave. This is useful for adjusting the phase of the output after the 440A has obtained lock. Factory default is N=0. |
| C x | **E**nable (x=E) or **D**isable (x=D) external lock. When disabled, the internal TCXO is used without locking to an externally supplied clock. |
| E x | Serial Echo Control. x=D for Echo **D**isable, x=E for Echo **E**nable. Default is **E**nabled. |
| T x | ECL Output Control. x=D for ECL **D**isable, x=E for ECL **E**nable. Default is **D**isabled. (requires internal configuration) |
| S | Save current state into EEPROM and sets the EEPROM valid flag. The state saved is used as default upon next power up or reset. |
| STOP | Turns off the internal microprocessor. The "STOP" command automatically saves all present settings. Use this command in embedded applications for lowest system noise and power. A logic low (open collector) pulse must be applied to the CLR_STOP* connector pin to restore normal operation. After a CLR_STOP* pulse, factory defaults are restored. (an internal on-board push button implements the "CLR_STOP*" pulse) |
| R | Reset. This command resets the unit. EEPROM data is preserved and, if valid, it is used upon restart. This is the same as cycling power or toggling the open collector RES* line on the connector. (an internal on-board push button implements a "RES*" pulse) |
| CLR | Clear. This command clears the EEPROM valid flag and restores all factory default values. |
| QUE | Read present frequency, phase and status. Returns a character string of internal settings, lock status and software revision number. Hexadecimal format. See operating notes for details. |